## Physics 310

## Lab 9-ADC and DAC

## General Procedures:

The circuit used involves a large number of connections so it has been wired permanently. The diagrams for the ADC and the DAC are shown on the last page. The connectors for the power supplies, clock pulse, input, and output are marked. Be careful not to apply to much pressure on the circuit board when attaching the cables to it. There are switches between the outputs of the ADC and the inputs of the DAC so that the DAC can be disconnected and used independently.
A digital probe will be used to check the states of digital outputs. Its black clip should be connected to ground and its red clip to +5 V . Set the switches on the probe to PULSE and CMOS. When the tip is touched to a logic output, the LEDs will indicate its state.

## 9-1. ADC

A. The ADC 0809 is set up to convert voltages from 0 to +5 V into 8 -bit binary by connecting $\mathrm{V}_{\text {REF }}$ to ground and $\mathrm{V}_{\text {REF }}{ }^{+}$to +5 V . It will convert negative voltages as if they were zero. The circuit is constructed in free-running mode, which means that the once it is done converting the result is output and another conversion is started. This is done by connecting the output enable (OE) to 5 V , the clock (CLK) to the address latch enable (ALE), and the end of conversion (EOC) to Start. AD A, AD B, and AD C are grounded to select input 0 (IN 0 ). All of the unused inputs are also grounded.
B. The ADC0809 needs a clock input to step it through the conversion process. Use the TTL/CMOS output of a function generator with the knob pulled out for CMOS and adjusted so that the HIGH value of the pulse is +5 V . Set the frequency of the clock pulse to 100 kHz .
C. Make sure all eight of the switches are set to ON so that the outputs of the ADC are connected to the inputs of the DAC. The outputs of the ADC can be tested at the input pins for the DAC with a digital probe. Input an adjustable DC voltage into the ADC and record the output state in 0.5 V increments between 0 and +5 V .
Question: How do the outputs of the ADC compare to what you expect?
D. While watching the least significant bit (LSB) of the ADC output, slowly adjust the DC voltage and determine what voltage change causes this bit to switch states. Since the voltage change is small, make the LSB to switch ten or more times and average the voltage changes required for each switch (in either direction).
Question: How does the voltage change required to switch the state of the LSB compare to what you expect?
E. Look at the clock pulse and the end of conversion (EOC) signal from the ADC on an oscilloscope. Trigger on the EOC.
Questions: How many clock pulses are there between EOC pulses? Is this what you expect? Explain.

## 9-2. DAC

A. The DAC0800 converts an 8 -bit, digital input into an analog output.
B. Set all eight of the switches to OFF so that the DAC is separated from the ADC.
C. Set all of the inputs to the DAC to LOW and measure the voltage of the output to determine the minimum output voltage. Change all of the inputs to HIGH to determine the maximum output voltage.
Question: Over what range does the output vary?
D. Input HIGH $(+5 \mathrm{~V})$ to the LSB and LOW (ground) to the rest of the bits, then measure the output. Measure the output with the input to each individual bit HIGH and the rest of the bits LOW.
Question: Are the outputs what you expect? Show your calculations.
E. Calculate the digital input required to get an output as close as possible to +3 V . Test the result of this input.
Question: How close is the output to +3 V?

## 9-3. Combined ADC and DAC

A. Set all eight of the switches to ON to reconnect the ADC and DAC. With the clock frequency set to 100 kHz , input a $100-\mathrm{Hz}, 4-\mathrm{V}$ peak-to-peak sine wave centered around +2.5 V and observe the output.
Question: How accurately does the output reproduce the input?
B. Observe what happens to the output as the clock frequency is reduced.

Questions: At what sampling frequency does the output no longer have the same frequency as the input? Does this agree with the Nyquist criterion?


* NOT三: $i$ NEDSS TO TBE 2 mA , THEREFOR, for $~ V+=+15, R_{1,2}=7.5 \mathrm{k}$ $\omega / R 1=R 2$.

$$
+12, R_{1,2}=6.0 \mathrm{k}
$$

$+10, R_{1,2}=5.016$

$$
\frac{\text { etc. }}{L \equiv T|v+|=| v-1} \begin{aligned}
& \\
& \\
& \\
& \pm 15 \\
& \text { etc. }
\end{aligned}
$$

Layout of the circuit board (in case the labels come off).


