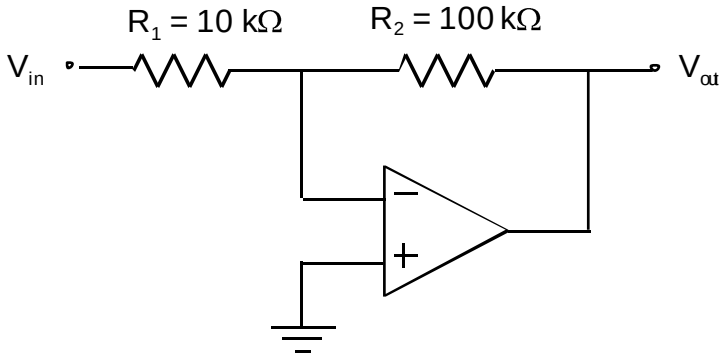
2nd Exam Sample Problems (remember, there's also a multiple-choice comprehensive part covering R, C, and L; no equation sheet for that part)

Golden Rules for Ideal Op Amps with negative feedback:

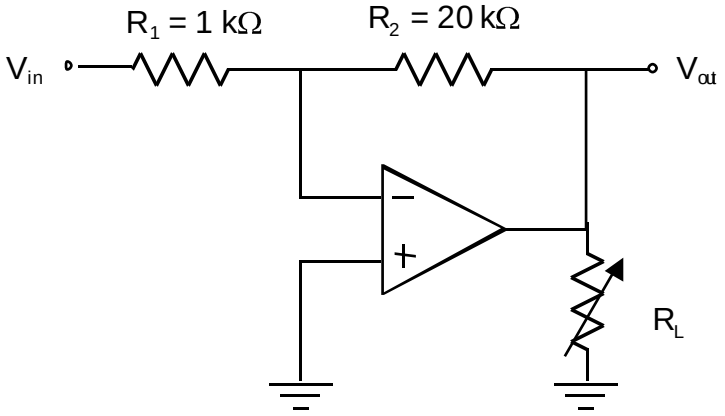
1. The output will adjust in any way possible to make the inverting input and the non-inverting input terminals equal in voltage.
2. The inputs draw no current.

1.



For the op amp circuit above, how is the output voltage related to the input voltage?

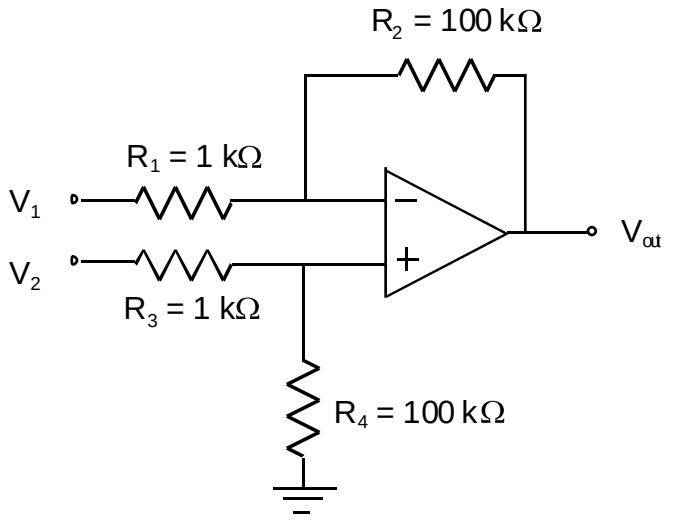
2.



For the op amp circuit above, how is the output voltage related to the input voltage?

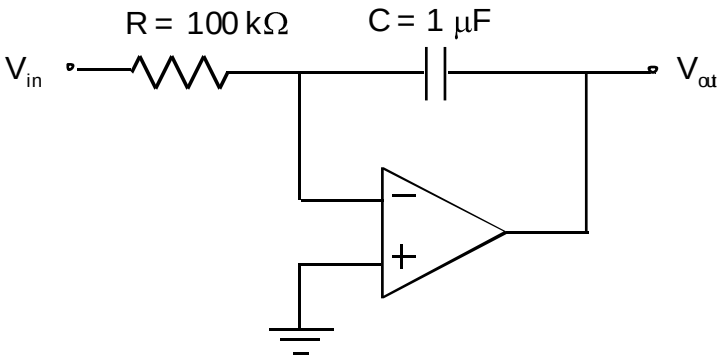
2nd Exam Sample Problems (remember, there's also a multiple-choice comprehensive part covering R, C, and L; no equation sheet for that part)

3.



For the op amp circuit above, how is the output voltage related to the input voltages?

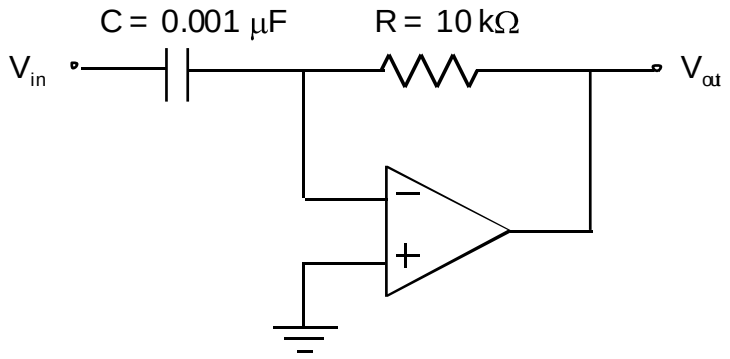
4.



Suppose that the input voltage for the circuit above is 10-V peak square wave with a frequency of 250-Hz. Carefully sketch (including scales) the output voltage versus time.

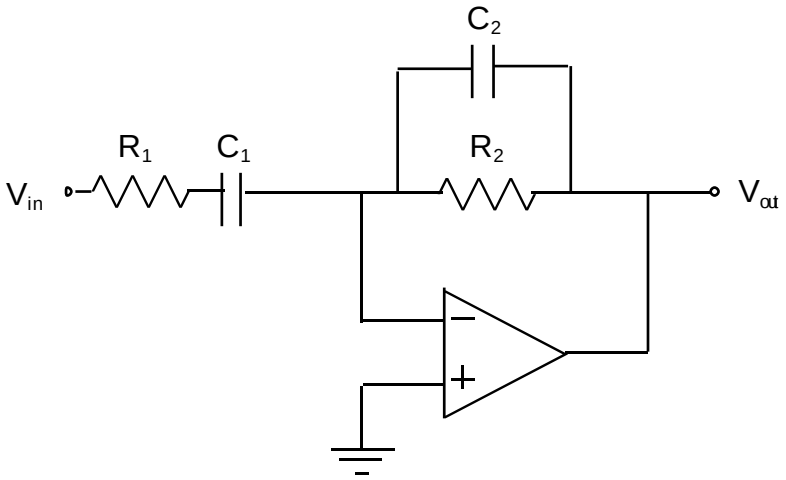
2nd Exam Sample Problems (remember, there's also a multiple-choice comprehensive part covering R, C, and L; no equation sheet for that part)

5.



Suppose that the input voltage for the circuit above is 10-V peak triangular wave with a period of 4 ms. Carefully sketch (including scales) the output voltage versus time.

6.



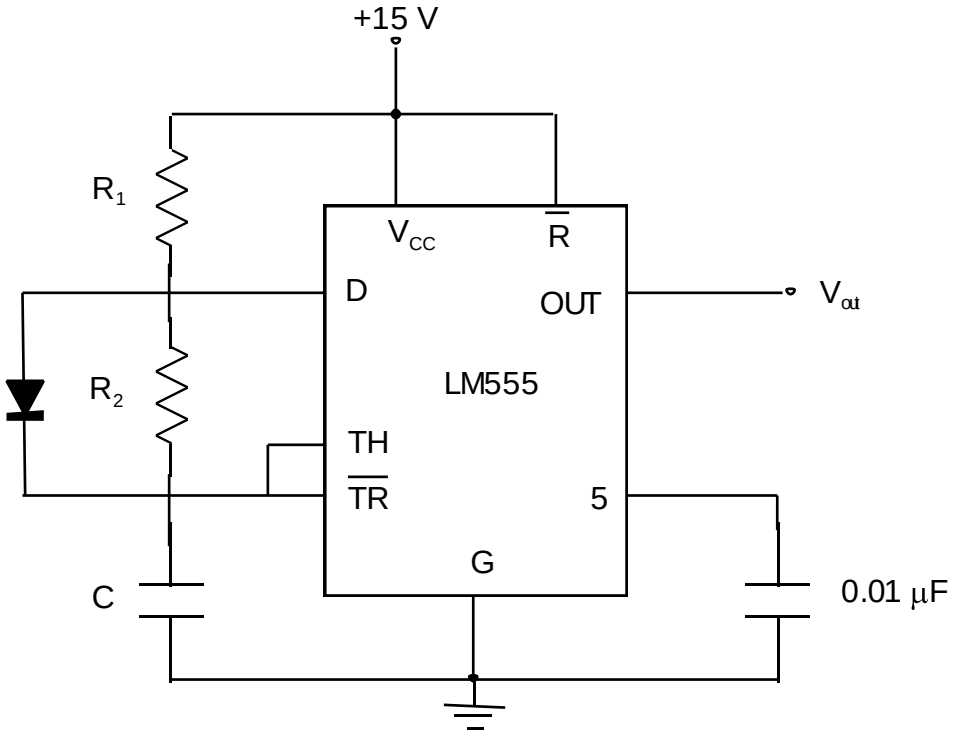
For the op amp circuit above, sketch the gain as a function of the frequency of the input signal.

7. Design a timing circuit that will produce a "square" wave that will have an output that is high for 100 ms and low for 5 ms.

2nd Exam Sample Problems (remember, there's also a multiple-choice comprehensive part covering R, C, and L; no equation sheet for that part)

8. Design a timing circuit that will produce a "square" wave that will have an output that is low for 10 ms and has a duty cycle of 40%.

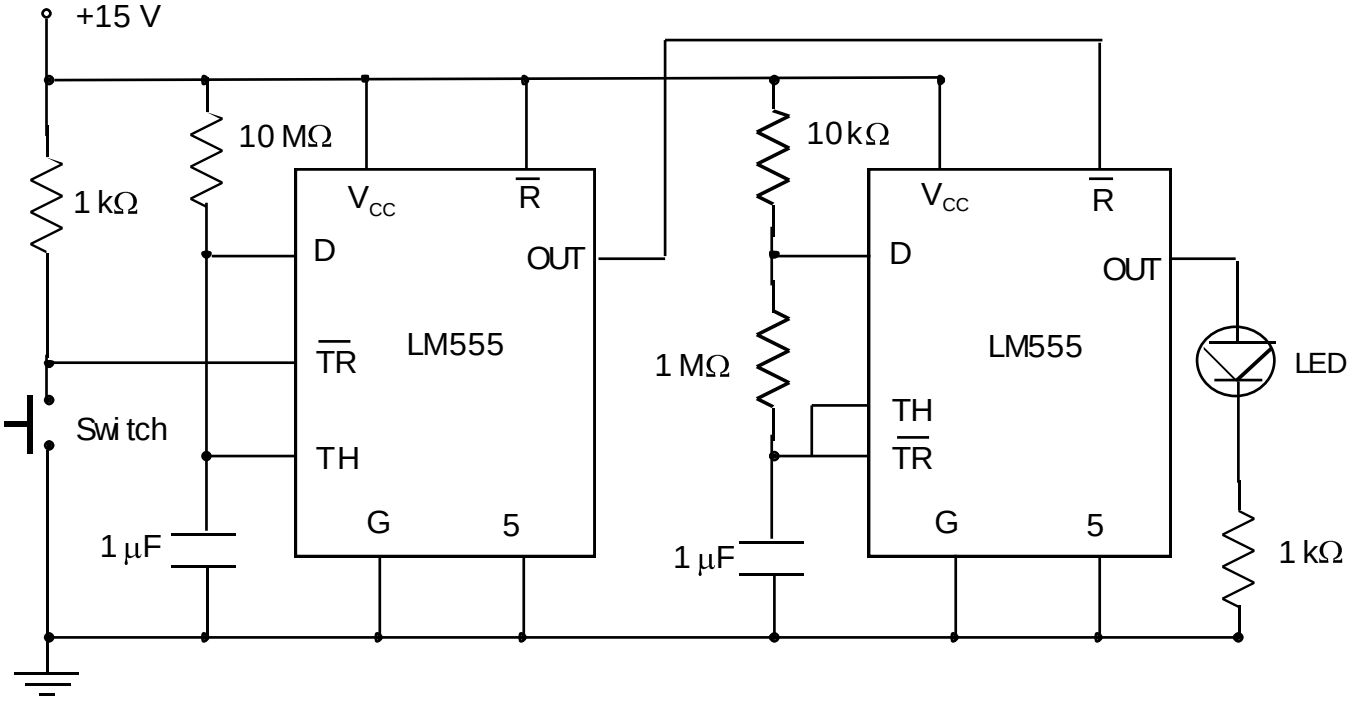
9. Suppose a diode is connected in parallel with R_2 of an astable oscillator made with a 555 timer IC as in the circuit below (taken from the Nov. 2003 issue of *Nuts & Volts*).



How will the diode change the operation of the circuit?

2nd Exam Sample Problems (remember, there's also a multiple-choice comprehensive part covering R, C, and L; no equation sheet for that part)

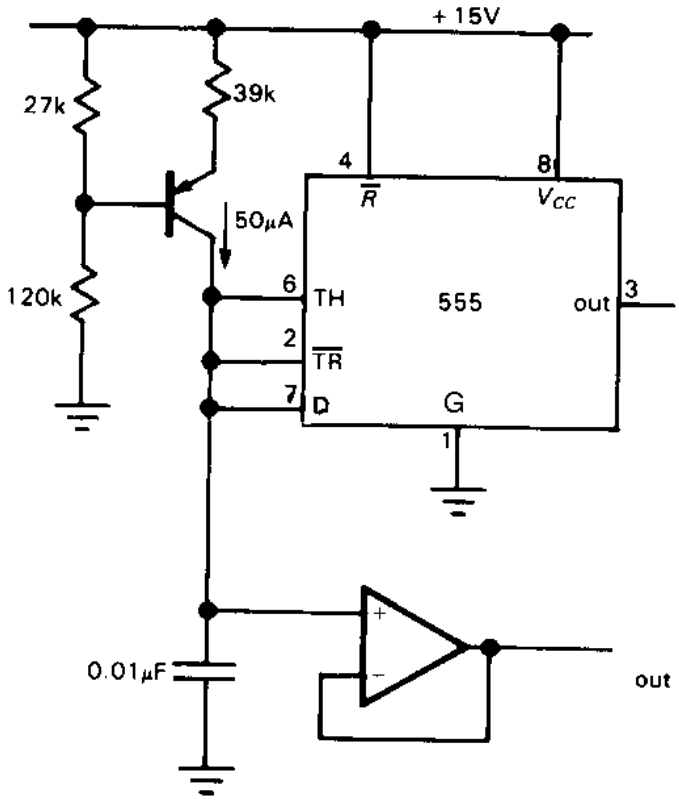
10. In the circuit below (taken from the Nov. 2003 issue of *Nuts & Volts*), wires are not connected everywhere they cross, only where they are marked.



What does the circuit do after the switch is pushed? Be very specific.

2nd Exam Sample Problems (remember, there's also a multiple-choice comprehensive part covering R, C, and L; no equation sheet for that part)

11. The pnp transistor in the circuit below (taken from *The Art of Electronic* by Horowitz and Hill) provides a constant current of 50 μA.



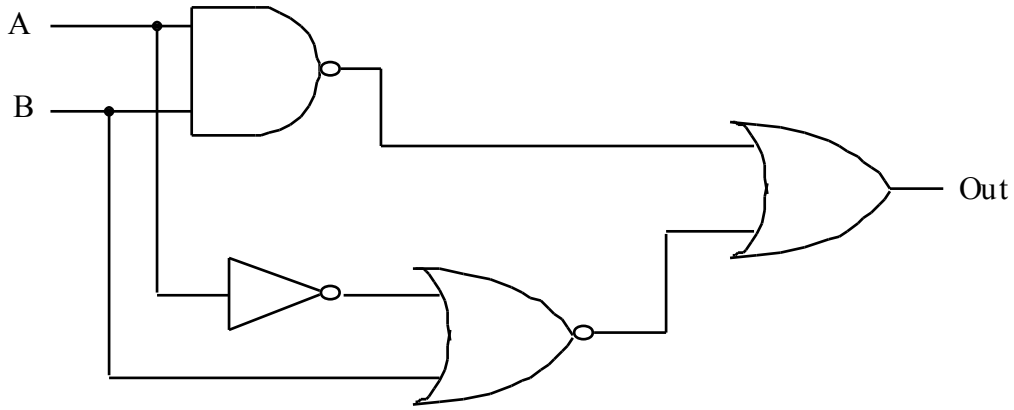
a) What is the output of the op amp?

b) What is the output of the 555 IC?

c) Why is the op amp necessary?

2nd Exam Sample Problems (remember, there's also a multiple-choice comprehensive part covering R, C, and L; no equation sheet for that part)

12. Complete the truth table for the following circuit. Note that the wires that cross are <u>not</u> connected.

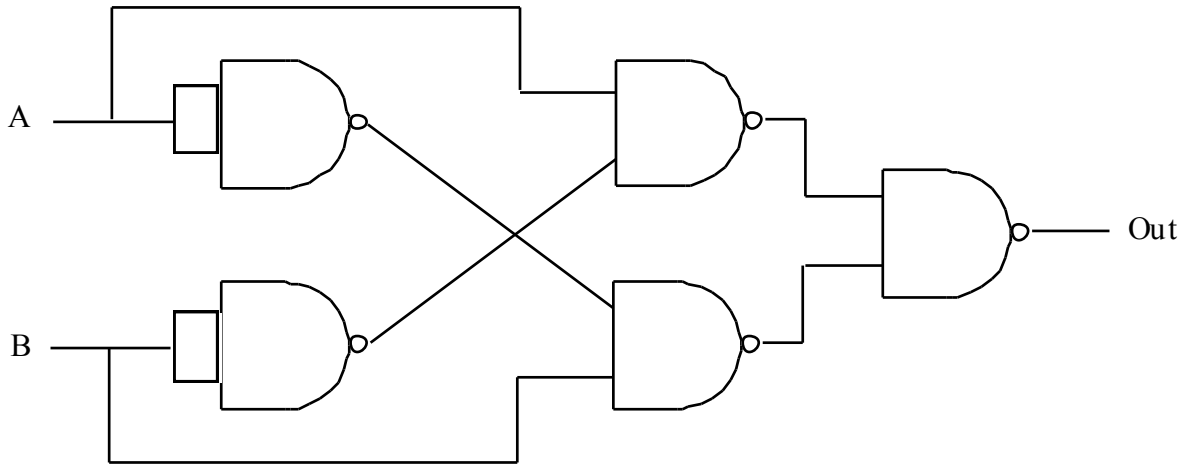


A	B	Out
0	0	
1	0	
0	1	
1	1	

What logic function does this circuit perform?

2nd Exam Sample Problems (remember, there's also a multiple-choice comprehensive part covering R, C, and L; no equation sheet for that part)

13. Complete the truth table for the following circuit. Note that the wires that cross are <u>not</u> connected.

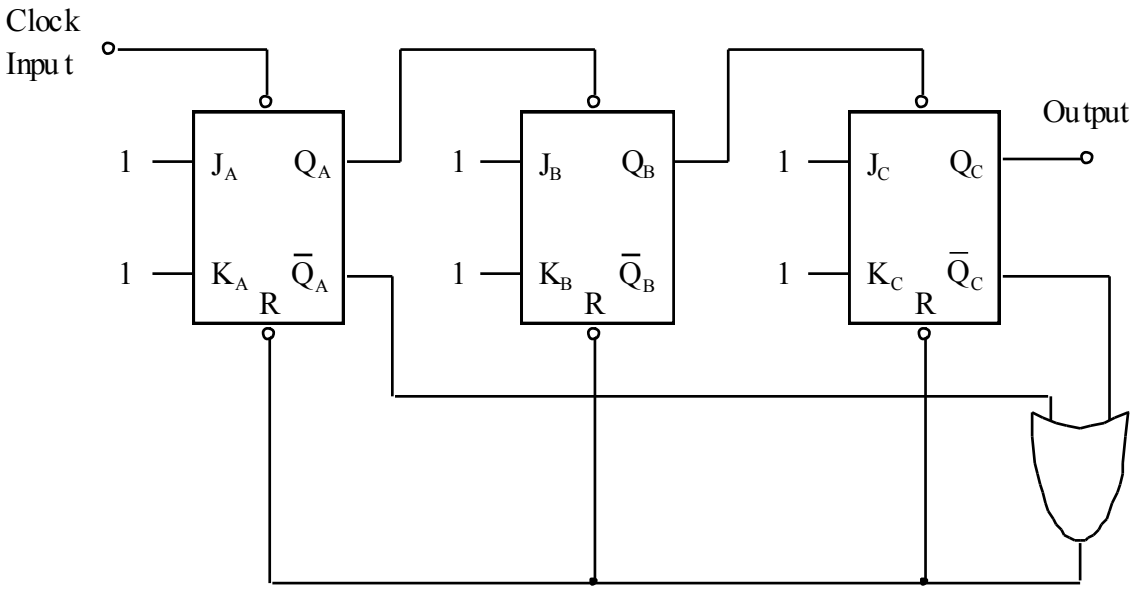


A	B	Out
0	0	
1	0	
0	1	
1	1	

What logic function does this circuit perform?

2nd Exam Sample Problems (remember, there's also a multiple-choice comprehensive part covering R, C, and L; no equation sheet for that part)

14. Assume that the J-K flip-flops are in an initial state with $Q_A=Q_B=Q_C=0$. Analyze the behavior of the circuit below by filling in the truth table for subsequent clock pulses. Stop when the circuit returns to its initial state (for three J-K flip-flops, the maximum number of states is 8). Note that where wires cross they only connect if there is a dot.

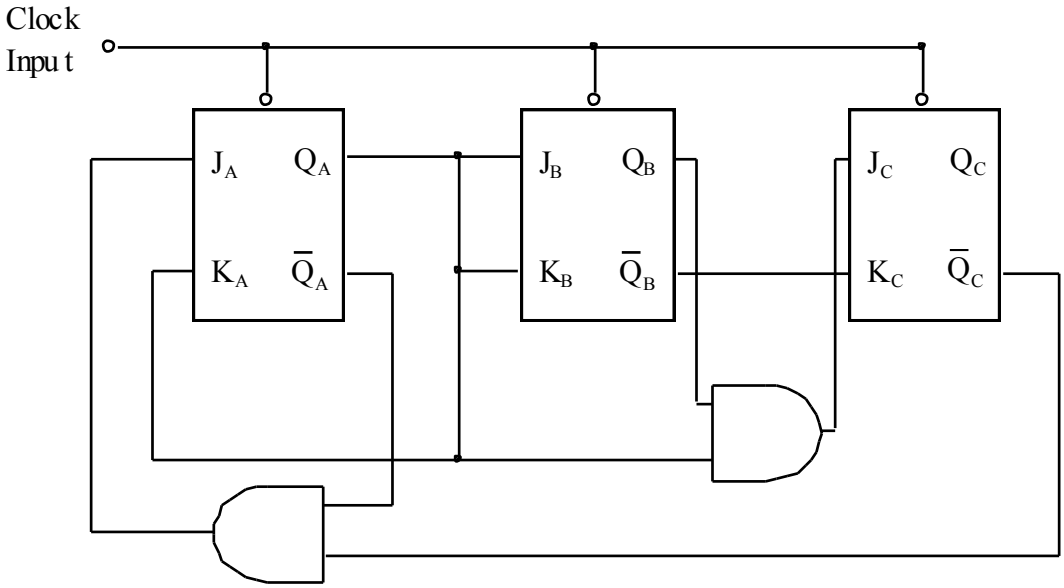


State	Q_A	Q_B	Q_C
1	0	0	0
2			
3			
4			
5			
6			
7			
8			

If Q_C is considered the output, what is the function of this circuit?

2nd Exam Sample Problems (remember, there's also a multiple-choice comprehensive part covering R, C, and L; no equation sheet for that part)

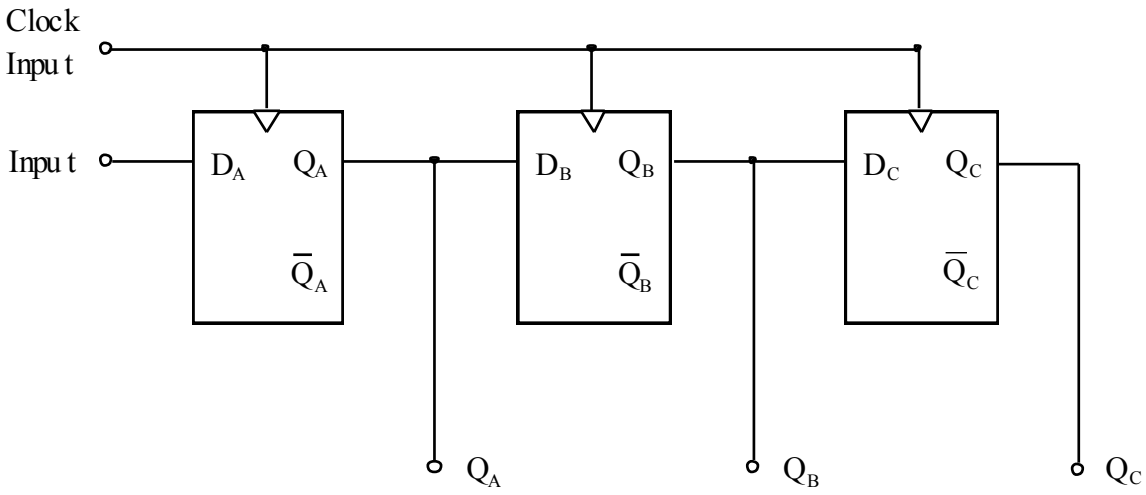
15. Assume that the J-K flip-flops are in an initial state with $Q_A=Q_B=Q_C=0$. Analyze the behavior of the circuit below by filling in the truth table for subsequent clock pulses. Stop when the circuit returns to its initial state (for three J-K flip-flops, the maximum number of states is 8). Note that where wires cross they only connect if there is a dot.



State	Q_A	Q_B	Q_C
1	0	0	0
2			
3			
4			
5			
6			
7			
8			

2nd Exam Sample Problems (remember, there's also a multiple-choice comprehensive part covering R, C, and L; no equation sheet for that part)

16. Analyze the behavior of the circuit below by filling in the truth table for 5 subsequent clock pulses. Note that data flip-flops are used. Assume that its initial state is $Q_A=Q_B=Q_C=0$ and that the input (D_A) is "1" for the first clock pulse, then "0" for all of the others.



State	Q_A	Q_B	Q_C
1	0	0	0
2			
3			
4			
5			
6			

What use might this circuit have?

2nd Exam Sample Problems (remember, there's also a multiple-choice comprehensive part covering R, C, and L; no equation sheet for that part)

17. A 6-bit, successive-approximation ADC has an input range of 0 to 10 V and has a clock frequency of 10-kHz. The output of the ADC is connected to a 6-bit DAC with an output range of 0 to 10 V.

(a) What increment in the input will cause a 1-digit change in the output of the ADC?

(b) How long does it take the ADC to make one conversion?

(c) What is the output from the ADC when the input is 4.5 V?

(d) What is the output from the DAC when the input to the ADC is 4.5 V?

(e) What frequencies will be reasonably well reproduced by this circuit?