Physics 310
Errata for *Principles of Electronic Instrumentation*, Third Edition
by Diefenderfer and Holton - updated 04/08/08

p. 2: The labels for the earth ground and chassis ground symbols are not consistent with the inside of the front cover (but there is no universally accepted convention anyway.)

p. 11: The current through R_3 is $I_3 = I_1 – I_2 = 14.0$ mA – (–1.3 mA) = 15.3 mA, not 12.7 mA as the text states.

p. 15: The values of the components for Fig. 1.19 are missing, but appear on the next page in Fig. 1.20 except $R_5 = 2\ \Omega$.

p. 16: In Fig. 1.20, the second circuit diagram should not have the label "V_{TH}" across the open terminals because it is being used to determine R_{TH}. The first circuit diagram is used to find V_{TH}. In the fourth diagram, $R_5 = 2\ \Omega$, which is implied in the text.

p. 16: In Eqn. (1-34), some printings of the book have the voltage in the equation as "0.25" rather than "25".

p. 17: In Fig. 1.21, the label "V_0" should be changed to "V_L" which is the voltage across the load resistor. V_0 is the voltage in the limit that the load resistance is very large or $V_0 = \lim_{R_L \to \infty} (V_L)$.

p. 27: Equation (2-7) for finding the equivalent capacitance for capacitors in series should be $1/C_S = 1/C_1 + 1/C_2 + 1/C_3 = \Sigma(1/C_i)$.

p.27: in fig 2.4, the three polar capacitors should all have the same orientation; presumably C_3 is the one that's backwards.

p.29: "v" in Fig. 2.9 is the same as "v_b" in the equations on the same page.

p. 35: In Fig. 2.17, the voltage across the resistor (v_R) should start changing at the sametime as the voltage across the inductor (v_L).

pp. 44-5: The words defining the phase angle are good, but equation (3-4) should be $v(t) = V_P \sin(wt + f)$ in order to be consistent (and to match the definition of phase angle for phasors). The sign should be changed throughout Example 3.1, so the result for that should be $\phi = +90°$ (a cosine wave leads a sine wave).

p. 46: The equation between (3-7) and (3-8) should be: $I_{rms} = \sqrt{\frac{1}{T}\int_0^T I_p^2 \sin^2 wt\, dt}$.

p. 48: Since ωt is in radians, the phase angle should also be in radians, not degrees, so $f = \frac{p}{2}$ rather than 90°.

p. 51: Equation (3-28) should be $\mathbf{Z}_c = \ldots = |X_C| \angle -90°$ because the magnitude should be positive.

p. 52: Following the rule dividing phasors in equation (3-26), two equations in the analysis of the low-pass filter should be:

$$\boldsymbol{i} = \frac{V_{in}}{Z} \angle -\tan^{-1}(X_C/R) \qquad (3-35)$$

$$\boldsymbol{V_C} = \frac{V_{in}}{Z} \angle -\tan^{-1}(X_C/R) \times |X_C| \angle -90° \qquad (3-37)$$

Also, the magnitude of the result should be positive, so equation (3-38) should be:

$$\boldsymbol{V_C} = \left(\frac{V_{in}|X_C|}{Z}\right) \angle \left(-\tan^{-1}(X_C/R) - 90°\right)$$

and equation (3-40) should be: $\mathbf{V}_C = V_{out} = \frac{V_{in}|X_C|}{Z}$

p. 53: The first line of equation (3-41) should be A =…= $|X_C|/Z$.

p. 54: The standard definition of a ratio's decibel measure is $A_{dB} = 10dB\log_{10}(A)$ not $A_{dB} = 20dB\log_{10}(A)$ as the text strongly implies. What's approximately equal to 3dB at f_B is not the voltage gain (called A by this text), but the power gain, (which I'll call B), where B = A^2. So $B_{dB} = 10dB\log_{10}(B) = 10dB\log_{10}(A^2) = 20dB\log_{10}(A)$.

p. 55: Equation (3-50) should be $Z = \sqrt{R^2 + \left(|X_L| - |X_C|\right)^2}$ (the absolute values are missing).

p. 62: Equation (4-3) should be $i_p v_p = i_s v_s$.

p. 65: If the "source voltage" means that across the ideal AC supply (not that across the primary), then the voltage across the primary v_p should be half of the source voltage, since the impedance seen across the transformer is matched to internal resistance of 4.9 k-ohms. The secondary voltage should be v_s = 2 V, so the secondary current is i_s = 20 mA and the power is P_s = 40 mW.

p. 86: In the third circuit in Fig. 5.15, the transformer should have a center tap connected to ground.

p. 98: In problem 3, the 100-Ω resistor will be damaged even if the load resistor is not removed since the power is $(6.9\text{ V})^2/(100\ \Omega) = 0.48$ W. This would not be true if it were a 1/2-W resistor.

p. 165: Equations 8-23 and 8-24 aren't quite consistent with the notation used in 8-22; to be consistent, b^2 should just be b (overall), i.e., $b_1 b_2$.

p. 167: In Fig. 8.15 B, there should be no connection between the Gate (G) and Source (S) terminals of the JFET. Also, the depletion zone doesn't lengthen toward S, it widens into the channel, making the channel narrower. If anything, it slightly lengthens toward D since it's more reverse biased with respect to D.

p. 185: The more formal analysis of op amps is in Appendix B-2, not Appendix A.

p. 224 & 225: in figure 10.14 and accompanying text at the top of p. 225, the frequency is $f = \frac{1}{2RC\ln(2)}$ which *isn't* terribly well approximated as $f \approx \frac{1}{2RC}$.

p. 227: Equation (10-17) for the duty cycle should be $D.C. = t_2/(t_1 + t_2) = R_2/(R_1 + 2R_2)$.

p. 229: The ICL8038 function generator gives more symmetric output if separate resistors are used between pin 4 and V_+ and between pin 5 and V_+. If the same resistances are used, the output frequency will be $f = 0.33/RC$.

p. 230: The data sheets for the ICL8038 are missing from Appendix D.

p. 253: In table 11.12, the headings for the hexidecimal and binary columns are swapped.

p. 254: The circuit in Fig. 11.22 doesn't operate as advertised. If both inputs to either NAND are Hi, then that NAND's output is a current sink, pulling the output line Low, regardless of whether there's a Low input to the other NAND. To have the function advertised, use two AND's and then invert the final output line.

p. 261: In Figure 12.1, the truth table is should be in terms of $\bar{S}$ and $\bar{R}$ since they are the actual inputs to the flip-flop.

p. 276: The text states that "Figure 12.22 illustrates this case for a synchronous divide-by-16 counter," but the circuit is a divide-by-10 counter.

In Figure 12.21, the labels "J_A", "K_A", etc. should not appear in the table. The first two states are repeated in the table. The caption refers to the circuit as a "divide-by-6" rather than a "divide-by-16" counter.

p. 278: In Figure 12.23, some of the J and K inputs of the flip-flops are left floating which is not a good idea. They should be kept HIGH. The "Clock in" should only connect to flip-flop A. The labels "J_A", "K_A", etc. should not appear in the table.

p. 279: In Figure 12.24, some of the J and K inputs of the flip-flops are left floating which is not a good idea. They should be kept HIGH.

p. 297: In Figure 12B, the J and K inputs of the flip-flop on the left should be kept HIGH to ensure that it changes state with every clock pulse. Also, this is the same as the circuit in Figure 12.21 which is used as an example in the chapter.

p. 306: The 78184 (BCD to binary) and 78185A (binary to BCD) chips have been discontinued.

p. 349: In the description of the successive-approximation ADC, the output of the DAC should be compared to the analog input (not the reference voltage for the DAC).

p. 350: In Table 14.5, the rightmost column should be labeled “LSB”, not “MSB.”

p. 351: In Figure 14.16, the analog input and the output of the DAC should go into different terminals of the comparator. Also, the digital outputs are usually buffered so they are only updated when the conversion is complete.

p. B-2: Equations (B-3) to (B-9) only apply if $R^2/4L^2 < 1/LC$.